Abstract—SystemC-AMS as an extension of SystemC provides the essential capability to describe a mixed-signal heterogeneous system, so that a virtual-prototype model can be generated to help analyze a whole mixed-signal system and further guide the circuit design. This paper presents a novel SystemC-AMS model of a high frequency Charge Pump Phase Lock Loop, including digital models like Phase/Frequency Detector and clock N-divider, and analog models like Charge Pump, Low Pass Filter and Voltage Controlled Oscillator. In order to prove the model's accuracy, the SPICE simulation result from the corresponding CMOS circuits based on the same structure of these models is used for comparison, and PLL SystemC-AMS model is validated.

Index Terms—SystemC-AMS, Charge Pump, PLL, CMOS

I. INTRODUCTION

When designing a high-speed mix-signal CMOS circuit, more complexity and unforeseen factors occur and it is not wise to analyze the performance after the layout design which takes a long time. SystemC-AMS as an extension of SystemC provides the essential capability to describe a mix-signal heterogeneous system [1], so that a virtual-prototype model can be generated to help analyze a whole mix-signal system and further guide the circuit design. To design a high-speed Charge Pump Phase Lock Loop (CP-PLL) is an example of proving SystemC-AMS as a function of the bridge between the high-level system analysis and the specified bottom CMOS design. To approach a more precise result about this CP-PLL model, the key components are described at a low level in SystemC-AMS while others are at a high level. To prove the veracity, the simulation from SystemC-AMS model has to be compared with the waveforms of the real CMOS circuit, and then some modifications to the model may be necessary.

II. CHARGE PUMP PHASE LOCK LOOP THEORY

A basic Phase Lock Loop (PLL) contains Phase/Frequency Detector (PFD), Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO). If PLL is used to multiply clock frequency, a clock divider is also included. A Charge-Pump PLL (CP PLL) inserts a charge pump between the PFD and LPF.

When there is a phase difference $\Phi$ by $\omega_1$ before $\omega_2$ at time $t=0$, then a boolean $UP=1$ with a width $\Phi T/(2\pi)$ as $T$ is $u_1$ period time. If a capacitor CP is adopted for LPF, the charging current $I_S$ will increase the voltage on the CP by $(Is/Cp)\Phi T/(2\pi)$ and while $\Phi$ keeps unchanged, then $u_d$ will respond approximately as a linear function with a constant slope. If $\omega_1$ is behind $\omega_2$, the same situation happens but with a negative slope.

Therefore the whole PLL can perform as a linear system and its closed transfer function can be attained according to Fig.3.

Fig. 2. Linear Function of PFD/CP/LPF

Fig. 3. A Closed Loop Transfer Function

III. SYSTEMC-AMS MODEL

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If \( C_g < 0.2C_p \) [3][4], 2nd order PLL can approximately analyze the performance of a 3rd-order PLL.

Then transfer function and some intermediate variables for a 2nd order PLL are shown below,

\[
H_{PLL}(s)_{open} = \frac{I_s}{2\pi} \left( R_p + \frac{1}{C_p} \right) \frac{K_{VCO}}{s}
\]

\[
H_{PLL}(s)_{closed} = \frac{I_s K_{VCO}}{2\pi C_p} \left( \frac{R_p C_p s + 1}{s^2 + \frac{I_s K_{VCO} R_p}{2\pi} s + \frac{I_s K_{VCO}}{2\pi}} \right)
\]

\[
\omega_n = \frac{I_s K_{VCO}}{2\pi C_p}, \quad \zeta = \frac{R_p C_p}{2} \omega_n
\]

Here \( \omega_n \) is the VCO natural angular frequency, and \( \zeta \) is the PLL damping factor.

Given \( K_{VCO} \) the VCO gain, \( I_s \) the (dis)charging current, At meantime since \( I_s K_{VCO} = 0 \) the poles of \( H_{PLL}(s)_{closed} \) are

\[
s_{1,2} = -\zeta \omega_n \pm \omega_n \sqrt{\zeta^2 - 1}
\]

Therefore, in the real design, only choose \( R_p \) and \( C_p \) carefully in order to make that \( \zeta \approx 1 \). If \( \zeta < 1 \) then the complex \( S_{1,2} \) poles make PLL instable, and if \( \zeta > 1 \) then the convergence time will be long and the locked status will be harder to be acquired.

### III. SYSTEMC-AMS MODELS FOR PLL

SystemC-AMS can describe a mixed signal system at a high level and also can provide a detail description about specified networks or at a register transfer level. The charge pump(CP) and low pass filter(LPF) are characteristic for a CP-PLL[6] and determine the performance of the whole PLL. To improve the accuracy, describe CP/LPF in detail in a low circuit level while other parts are abstracted at a high level.

#### A. Phase/Frequency Detector

According to the theory, the function of a PFD in CP-PLL is to detect the difference between the reference clock \( \omega_1 \) and the feedback clock \( \omega_2 \) and produces “UP = 1, DN = 0” when \( \omega_1 \) is ahead of \( \omega_2 \) or “UP = 0, DN = 1” when \( \omega_1 \) is behind \( \omega_2 \).

Based on Fig.3, the digital PFD is described in SystemC. The kernel idea here is to subtract \( \omega_1 = \text{ref} \) and \( \omega_2 = \text{fdbk} \) at the rising edge of either of input signals, and then certain pulse is generated when there is difference between 'ref' and 'fdbk'. A simulation result of this PFD is shown in Fig.6, which displays a consistent waveform as its theory.

```c
SC_MODULE(phd) {
    sc_in<bool>  ref,  fdbk;
    sc_out<bool> UP,  DN;
    double diff;
    void sig_proc() { ...  ...
        diff = ref_binary - fdbk_binary;
        if(diff > 0) {UP.write(true); DN.write(false); }
        else if (diff < 0) {UP.write(false);DN.write(true); }
        else{UP.write(false); DN.write(false); }     }
    SC_CTOR(phd) {
        SC_METHOD(sig_proc)
        sensitive_pos << ref;  sensitive_pos << fdbk; }
};
```

For its circuit counterpart, a classical structure[5][9] is adopted as Fig.7.

Comparing Fig.6 and Fig.7b, the main function is demonstrated the same, but there is an additional pulse with a width of around 250ps on UP or DN in the layout simulation when it’s zero in the SystemC abstracted simulation. This is caused by the intrinsic timing delay of a MOS DFF device, which will not influence the performance of the PFD but benefit its sensitivity[5]. To modified SystemC model purposely, the dotted line in Fig.6 can be generated.

#### B. Voltage Controlled Oscillator

The output frequency of VCO is determined by the input
controlled voltage \( V_c \) in Fig. 1. Defining VCO linear dynamic range \( \Delta f \), its central frequency \( f_0 = 2 \pi \omega_0 \), and the range of its controlled voltage \( \Delta V_c \), then

\[
K_{VCO} = \frac{\Delta f}{\Delta V_c} \quad \text{[Hz/V]}, \quad f_{VCO} = f_0 \pm \frac{\Delta f}{2}
\]

Considering \( V_c \in [0.1, 0.5] \), \( f_0 = 1.25 \text{GHz} \) and \( \Delta f = 500 \text{MHz} \) as the dotted line in Fig. 8 and . After the circuit design as Fig. 10, actually \( V_c \in [0.09, 0.4] \) and \( \Delta f = 470 \text{MHz} \) then \( K_{VCO} = 1.48 \times 10^9 \text{[Hz/V]} \). Then The SystemC-AMS code in the abstracted level for this VCO is attached below.

A simulation of this VCO SystemC-AMS model when controlled voltage \( V_c = 0.3 \text{V} \) is shown in Fig. 9, and the sine wave here is the VCO output before a shaping operation.

For its circuit counterpart, an analog 3-stage differential VCO [14][15] is used in Fig. 10.

A simulation based on the RC-extracted SPICE netlist from VCO layout shows the same as Fig. 9 and an expected 1.25GHz output with the central controlled voltage \( V_c = 0.31 \text{V} \).

C. Clock Divider

A clock divider is an optional element in Fig. 1 for a CP-PLL, but when CPPLL is aimed to multiply the clock frequency, a clock divider must be involved. When \( N = 10 \), a 125MHz reference clock is needed while VCO output 1.25GHz.

D. Charge Pump and Low Pass Filter

A basic Charge-Pump is shown in Fig. 1, but a significant shortcoming of the 3rd-order CPPLL is that there is a voltage drop on the resistor \( R_p \) which causes impulses on the controlled voltage of VCO. To compensate this, an equipotential connection is one solution [5][7][8] shown in Fig. 12, where SystemC-AMS network model is attached.

The above SystemC code is for this 1/10 divider, and its simulation is shown in Fig. 11.
Here $I_s=20\mu A$ is assumed, and $N=10$, $K_{VCO}=1.48 \times 10^9 \text{Hz/V}$ are known. Considering $C_p=8$pf and $R_p=10k\Omega$, then PLL damping factor: $\zeta = 0.769 \approx 1$.

Fig.13 shows the simulation result of CP-LPF model, from which a smooth rising or falling on the controlled voltage ($V_c$) is seen.

Fig. 13. CP-LPF SystemC-AMS Model Simulation

As mentioned before, this part is described in a low level in SystemC-AMS, and its circuit counterpart adopts the same structure as Fig.14 and the simulation keep as same as Fig.13.

Fig. 14. CP-LPF CMOS Circuit

E. Integration of CP-PLL

So far, all the components in this CP-PLL are introduced and here they are integrated into a loop. Under the condition that $C_p=8$pf, $R_p=10k\Omega$, $I_s=20\mu A$, $N=10$ and $K_{VCO}=1.48 \times 10^9 \text{Hz/V}$, with a 125MHz reference clock input, a SystemC-AMS model is shown below and its simulation is shown as Fig.16aTo compare the performance of the whole loop, its circuit counterpart is also designed in 130um CMOS process as Fig.15, and the simulation of its RC-extracted SPICE netlist of CPPLL CMOS layout is shown as Fig.16b.

Fig. 15. CP-PLL CMOS Circuit Layout

Comparing this waveforms and Fig.16a and b, they prove the same function as PLL, but with several differences.

Fig.16  CP-PLL Simulation

<table>
<thead>
<tr>
<th>Time</th>
<th>0 ns</th>
<th>100 ns</th>
<th>200 ns</th>
<th>300 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>DN</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>UP</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Vc</td>
<td>0.31</td>
<td>0.31</td>
<td>0.31</td>
<td>0.31</td>
</tr>
<tr>
<td>ref</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>vco_di</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>vcoo</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. SystemC-AMS Model Simulation

b. CMOS Circuit Simulation

Fig.16 CP-PLL Simulation
The rudimental pulse on UP/DN signal was explained before and can be kept the same at high level description in SystemC-AMS.

But a significant distinctness between SystemC-AMS model and the CMOS circuit result is the locked time of CPPLL which is inflected from the waveform of the controlled voltage Vc. In fact the locked time is determined by its damping factor $\zeta$, and this $\zeta$ is influenced by $R_p$ and $C_p$, that was discussed in former section. In our CMOS circuit design, a polysilicon rectangle is to realize the resistor and a PMOS junction capacitance is to realize the capacitor, then it is hard to produce a precise resistor and capacitor with low costs, because the values of these $R_p$ and $C_p$ depend on the CMOS process parameters which vary along with many factors like temperature. And also the parasitical RC parameters in the CMOS layout and devices will influence change $R_p$ and $C_p$ too. Therefore it is improbable to make the locked time of a SystemC-AMS model at a high level and the locked time of this CMOS circuit exactly the same all the time. However their locked times are in the same time-level, of around from 400ns to 800ns, and this is enough for a system designer. Another difference is the initial status of these two simulations. For SystemC-AMS model, it’s deterministic at the initial stage but for a mixed-signal CMOS circuit, it’s hard to attain all its initial status although the SPICE simulation can set initial point for its netlist. However this difference doesn’t influence the performance of the PLL.

From a high level, the SystemC-AMS model is considered to be the same as its CMOS circuit counterpart at the interface when PLL is stable.

IV. Off-chip Test Model

High frequency output should be tested through certain wired channel, so an off-chip test model in SystemC-AMS is needed sometimes. Paper[19] gave an insight reference to model the channel in Systemc-ams, and further provided a method to transfer the standard IBIS model of the package into a Systemc-ams file. And report[20] provided information about how to deal with an IBIS model for high-speed LVDS interface.

In this paper a basic LVDS driver and a symmetrical segment for the distributed double-wire model with simple package model are described as Fig.17.

On the wire channel, the self-resistance $R$, self-capacitance $C$, self-inductance $L$ and the mutual-capacitance $C_{coup}$ on a Printed Circuit Board(PCB) are calculated[21] as below, while the mutual-inductance is ignored:

$$R = 0.641 \frac{l}{\omega} [m\Omega], \quad C = 0.0885 \frac{\omega}{H} [pF/cm]$$

$$L = 0.002 \ln \frac{8T + \frac{\omega}{4T}}{\omega} [\muH/cm],$$

$$C_{coup} = \frac{0.0885 \pi}{\cosh \left(\frac{D}{T}\right)} [pF/cm]$$

Here $T$ is the wire thickness, $H$ is the height of this wire layer above the power/group plane, $w$ and $l$ are the width and the length of the wires.

From this graph, it can be known that the performance gets worse when more channel segments are involved so that certain equalization circuits are needed before the LVDS driver if PLL outputs off-chip clocks.

V. Conclusion

A precise SystemC-AMS modeling for a CP-PLL is designed in detail, and its simulation is compared with the waveform from its CMOS circuit. Their consistency proves the accuracy of the CPPLL model when PLL is stable. A simple wired channel and LVDS driver in SystemC-AMS as an off-chip test model is also mentioned.

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REFERENCES