Et4054 Lab Session

given a number of circuits ...  

.... using a dedicated MATLAB toolbox  
    investigate the circuits with respect to scheduling, 
    retiming for minimum clock states, 
    design space exploration

For one of the scheduled circuits (still with the aid of the 
MATLAB toolbox),

    generate and execute a MATLAB testbench,  
    generate a VHDL testbench and simulate functional
    and timing behavior with ModelSim.

Optional: synthesize the VHDL design using Synplify Pro.
Toolbox written in MATLAB

• .... for scheduling (various scheduling methods, with/without resource constraints, resource latencies, etc)
• .... for retiming for minimum clock states,
• .... for obtaining Pareto points,
• .... for creating a MATLAB testbench and user-definable input sequences,
• .... for creating a VHDL architecture description and testbench
Figure 1.1  Block diagram of a 5th order FIR filter.

\[ y[n] = \sum_{i=0}^{5} c_i \cdot x[n - i] \]

Table 1.1  coefficients for the 5th order FIR filter

<table>
<thead>
<tr>
<th>( c_i )</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( c_0 )</td>
<td>-0.07556556070608</td>
</tr>
<tr>
<td>( c_1 )</td>
<td>0.09129209297815</td>
</tr>
<tr>
<td>( c_2 )</td>
<td>0.47697917208036</td>
</tr>
<tr>
<td>( c_3 )</td>
<td>0.47697917208036</td>
</tr>
<tr>
<td>( c_4 )</td>
<td>0.09129209297815</td>
</tr>
<tr>
<td>( c_5 )</td>
<td>-0.07556556070608</td>
</tr>
</tbody>
</table>
Table 1.1  coefficients for the 5th order FIR filter

<table>
<thead>
<tr>
<th>c₀</th>
<th>-0.07556556070608</th>
</tr>
</thead>
<tbody>
<tr>
<td>c₁</td>
<td>0.09129209297815</td>
</tr>
<tr>
<td>c₂</td>
<td>0.47697917208036</td>
</tr>
<tr>
<td>c₃</td>
<td>0.47697917208036</td>
</tr>
<tr>
<td>c₄</td>
<td>0.09129209297815</td>
</tr>
<tr>
<td>c₅</td>
<td>-0.07556556070608</td>
</tr>
</tbody>
</table>

Figure 1.2a  Magnitude transfer function of the 5th order FIR filter.
Figures 1.2 b and c. Time response of the FIR filter with the magnitude transfer function given in Figure 2a. The lower plots show the output time samples $y[n]$ for b) a unit impulse function as the input, and c) for a unit step function as input.
• obtain a sequencing graph that can be scheduled,

• scheduling software to show the influence of a couple of different scheduling methods,

• retiming algorithm: schedule the resulting circuit description(s)

• MATLAB to test the implementation which is derived from the scheduled graph (the SSG) in a fixed point environment,

• translate the scheduled circuit into a VHDL description,

• simulate this VHDL description using the ModelSim timing simulator
**ALU functions**

- **Add:** $y[n] = x_1[n] + x_2[n]$
- **Subtract:** $y[n] = x_1[n] - x_2[n]$
- **Constant multiplier:** $y[n] = k \cdot x[n]$
- **One clock cycle delay:** $y[n] = x[n-1]$
- **Negative of delay:** $y[n] = -x[n-1]$

*Figure 1.3  Explanation of the available basis elements.*
Introduction Lab Sessions ET4-054

different bus widths:
outside SSG
(N-M).M
inside SSG
((N-M+x).M)
N bits
(M+x) bits

feedback and ext I/O layer

Clk
Reset
Start
Done
Error

Coeficients

binar point aligned

(s)SG

feedback and ext I/O layer

Clk
Reset
Start
Done
Error

Coeficients

binar point aligned

(s)SG
Figure 1.1  Block diagram of a 5th order FIR filter.

Figure 1.4  Example of the labeling of the operations, inputs and outputs for the FIR5 filter.
Figure 1.6  Screenshot of schedGUI showing the Scheduled Sequencing Graph (SSG) for our FIR5 filter when a resource constrained List scheduling method has been applied.
Figure 1.7  Design space exploration for the FIR5 filter. It appears that for this particular (small) circuit – the schedules resulting from the ALAP and the Force Directed methods are exactly the same.

Figure 1.7 shows the results of executing `xplorere('FIR5.cir', [ 2; 1; 0.7 ]);`.
Data-flow graph obtained with view DFG('FIR5.cir'). A 'D' represents a Delay Element; 5D means 5 consecutive delays.
Retiming possible to decrease longest path to 3 state(s)

NOTE: Output will be delayed 1 additional 'sample' cycle(s)

Actions needed:
- Change 1T delay from i3 to v4 into a 2T delay.
- Change connection from v0 to s1 into a 1T delay.
- Change connection from v1 to s1 into a 1T delay.
- Change connection from v2 to s2 into a 1T delay.
- Change connection from v3 to s2 into a 1T delay.

Created file 'FIR5_3cyc.cir' for this retimed circuit ...
Table 1. *N*-bits integer representations (2’s complement for signed)

<table>
<thead>
<tr>
<th></th>
<th>value</th>
<th>range</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned</td>
<td>$N_{UINT} = b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \cdots + b_1s^1 + b_0s^0$</td>
<td>$0 \leq N_{UINT} \leq 2^{N-1}$</td>
</tr>
<tr>
<td>signed</td>
<td>$N_{SINT} = -b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \cdots + b_1s^1 + b_0s^0$</td>
<td>$-2^{N-1} \leq N_{SINT} \leq (2^{N-1} - 1)$</td>
</tr>
</tbody>
</table>

**Figure 2.** Fixed-point notation.
all coefficients are read from the .INP-file

50 ns

Clk

Reset

Nxt_InData = Start

Done

X clock cycles
depending on number of STATES

first input data value(s)
read from .INP-file

next value(s) read from .INP-file

output value(s) written to .OUT-file

start PASS 1, STATE 1

start PASS 2, STATE 1

Y clock cycles
depending on 'Sample Frequency'
5th Order Cauer (elliptical) filter

Magnitude in dB vs Frequency / Sample Frequency
Input Impulse Function

\[ x(n) \]

\[ y(n) \]

Impulse Response

Step Response

Input Step Function

\[ x(n) \]

\[ y(n) \]

Step Response

sample number

sample number
Start-up

Login with your NetId

MATLAB, ModelSim, Synplify_Pro

After starting MATLAB for the first time
folder ‘et4_054’ with all necessary data
file ‘ET4054_selection_for_<your NetId>’
(your personal selection for the assignment)

Note that you have to login and start MATLAB
at least once on one of the pc’s to obtain your ‘personal selection’.
Start-up (2)

• 1) Desktop PC in lab:
  • After login, press start, select ‘matlab et4054’; you will find a icon in your desktop, called Assignment2014….. that lists your 'personal assignment'.

• 2) Remote Desktop:
  • After command prompt type: % et4054_init, or % et4054_start